AMENDMENTS TO THE SPECIFICATION

Please amend the Specification as indicated below:

a. Kindly amend Paragraph **[0001]** as follows:

[0001] This application is a continuation-in-part of U.S. Patent Application No. 10/249,848, filed May 12, 2003, **now U.S. Patent 6,856,536,** which claims the benefit of U.S. Provisional Application No. 60/400,849, filed August 02, 2002, and U.S. Provisional Application No. 60/422,922, filed October 31, 2002, both of which are incorporated herein by reference in their entireties and for all purposes.

b. Kindly amend Paragraph **[0021]** as follows:

[0021] Conventional nonvolatile memory requires three terminal MOSFET-based devices. The layout of such devices is not ideal, usually requiring an area of at least $8f^2$ for each memory cell, where f is the minimum feature size. However, not all memory elements require three terminals. If, for example, a memory element is capable of changing its electrical properties (e.g., resistivity) in response to a voltage pulse, only two terminals are required. With only two terminals, a cross point array layout that allows a single cell to be fabricated to a size of $4f^2$ can be utilized. Co-pending U.S. patent application, "Cross Point Memory Array Using Multiple Thin Films," U.S. Application No. 10/330,512, filed December 26, 2002, **now U.S. Patent 6,753,561,** incorporated herein by reference in its entirety and for all purposes, describes such a device.

c. Kindly amend Paragraph **[0025]** as follows:

[0025] FIG. 1B depicts an exemplary stacked cross point array 150 employing four memory layers 155, 160, 165, and 170. The memory layers are sandwiched between alternating layers of x-direction conductive array lines 175, 180 and 185 and y-direction conductive array lines 190 and 195 such that each memory layer 155, 160, 165, and 170 is associated with only one x-direction conductive array line layer and one y-direction conductive array line layer. Although the top conductive array line layer 185 and bottom conductive array line layer 175 are only used to supply voltage to a single memory layer 155 and 170, the other conductive array line layers 180, 190, and 195 can be used to supply voltage to both a top and a bottom memory layer 155, 160, 165, or 170. Co-pending U.S. patent application, "Re-Writable Memory With Multiple Memory Layers," U.S. Application No. 10/612,191, filed July 1, 2003, **now U.S. Patent 6,906,939,** incorporated herein by reference in its entirety for all purposes, describes stacked cross point arrays.

d. Kindly amend Paragraph **[0029]** as follows:

[0029] FIG. 3 is a generalized diagrammatic representation of a memory cell 300 that can be used in a transistor memory array. Each memory cell 300 includes a transistor 305 and a memory plug 310. The transistor 305 is used to permit current from the data line 315 to access the memory plug 310 when an appropriate voltage is applied to the select line 320, which is also the transistor's gate. The reference line 325 might span two cells if the adjacent cells are laid out as the mirror images of each other. Co-pending U.S. patent application, "Non-Volatile Memory with a Single Transistor and Resistive Memory Element," U.S. Application No. 10/249,848, filed May 12, 2003, **now U.S. Patent 6,856,536,** incorporated herein by reference in its entirety for all purposes, describes the specific details of designing and fabricating a transistor memory array.

e. Kindly amend Paragraph **[0030]** as follows:

[0030] Each memory plug 255 or 310 contains a multi-resistive state element (described later) along with any other materials that may be desirable for fabrication or functionality. For example, the additional materials might include a non-ohmic device, as is described in co-pending application "High Density NVRAM," U.S. Application No. 10/360,005, filed February 7, 2003, **now U.S. Patent 6,917,539,** incorporated herein by reference in its entirety for all purposes. The non-ohmic device exhibits a very high resistance regime for a certain range of voltages (V_{NO-} to V_{NO+}) and a very low resistance regime for voltages above and below that range. The non-ohmic device, either alone or in combination with other elements, may cause the memory plug 255 or 310 to exhibit a non-linear resistive characteristic. Exemplary non-ohmic devices include three-film metal-insulator-metal (MIM) structures and back-to-back diodes in series.

f. Kindly amend Paragraph **[0031]** as follows:

[0031] Furthermore, as described in "Rewriteable Memory With Non-Linear Memory Element," U.S. Application No. 10/604,556, filed July 30, 2003, **now U.S. Patent 6,870,755,** incorporated herein by reference in its entirety for all purposes, it may also be possible for the memory cell exhibit non-linear characteristics without a separate non-ohmic device. It should be noted that since it is possible for a memory cell to exhibit non-linear characteristics the terms "resistive memory" and "resistive device" also apply to memories and devices showing non-linear characteristics, and can also be referred to as "conductive memory" and "conductive device." While a non-ohmic device might be desirable in certain arrays, it may not be helpful in other arrays.

g. Kindly amend Paragraph **[0034]** as follows:

[0034] As described in co-pending U.S. patent application, "A 2-Terminal Trapped Charge Memory device with Voltage Switchable Multi-Level Resistance," U.S. Application No. 10/634,636, filed August 4, 2003, **now U.S. Patent 7,038,935,** incorporated herein by reference in its entirety for all purposes, trapped charges are one mechanism by which the hysteresis effect is created. Trapped charges can be encouraged with dopants, as described in co-pending U.S. patent application, "Multi-Resistive State Material that Uses Dopants," U.S. Application No. 10/604,606, filed August 4, 2003, incorporated herein by reference in its entirety for all purposes.

h. Kindly amend Paragraph **[0035]** as follows:

[0035] It should be appreciated that fabrication of the multi-resistive state element might include additional techniques in order to ensure an effective memory device. For example, biasing the multi-resistive state element might be required in order to ensure the hysteresis is presented in a certain direction. Co-pending U.S. patent application, "Multi-Layer Conductive Memory Device," U.S. Application No. 10/605,757, filed October 23, 2003, **now U.S. Patent 6,965,935,** incorporated herein by reference in its entirety for all purposes describes using a multi-layered multi-resistive state element in order to encourage a hysteresis in a certain direction.

i. Kindly amend Paragraph **[0036]** as follows:

[0036] The fabrication techniques used for the memory plug 255 or 310 will typically dictate the requirements of the layers beneath the memory plug (e.g., in a transistor memory array the select line 320; and in a cross point array 100 or 150 the driver circuitry and conductive lines 105, 175, 180, 190 and 195). Since certain fabrication processes (e.g., solution based spin on followed by high temperature anneal, pulsed laser deposition, sputtering, and metal-organic chemical vapor deposition) might require high temperatures, refractory metals should be used for these layers so that they may withstand the temperatures. However, refractive metals have higher resistances, which may limit the number of cells on an array. Co-pending U.S. patent applications, "Laser Annealing of Complex Metal Oxides (CMO) Memory Materials for Non-Volatile Memory Integrated Circuits," U.S. Application No. 10/387,799, and "Low Temperature Deposition of Complex Metal Oxides (CMO) Memory Materials for Non-Volatile Memory Integrated Circuits," U.S. Application No. ~~**10/387,799**~~ **10/387,773** , both filed March 13, 2003, and both incorporated herein by reference in their entireties for all purposes, describe fabrication techniques that may be able to be used in lieu of high temperature fabrication processes.

j. Kindly amend Paragraph **[0048]** as follows:

[0048] Although the invention has been described in its presently contemplated best mode, it is clear that it is susceptible to numerous modifications, modes of operation and embodiments, all within the ability and skill of those familiar with the art and without exercise of further inventive activity. For example, each conductive plug might have a bottom surface area that is larger than the contact hole's top surface area such that each conductive plug has an overhang that is not in contact with the contact hole's top surface area. In such a case, a barrier layer that is in contact with the plug's overhang could be an advantageous improvement. Additionally, peripheral circuitry, such as that described in Co-pending U.S. patent application, "An Adaptive Programming Technique for a Re-Writeable Conductive Memory Device," U.S. Application No. 10/680,508, filed October 6, 2003, **now U.S. Patent 6,940,744,** incorporated herein by reference in its entirety for all purposes, can be easily implemented in the system. Accordingly, that which is intended to be protected by Letters Patent is set forth in the claims and includes all variations and modifications that fall within the spirit and scope of the claim.